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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/566,515
Filing Date: January 30, 2006
Appellant(s): SHRIVASTAVA ET AL.

Robert J. Crawford
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/20/08 appealing from the Office action mailed 11/29/07.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is essentially correct. Claims 1, 13, and 21 are independent and Applicant has essentially summarized the claimed subject matter for these independent claims. Examiner merely notes that the summary of claim 21, found on pages 3-4 of the Supplemental Appeal Brief of 5/20/08 (likewise in original Appeal Brief filed 4/28/08) contains an error,

characterized by the Examiner as typographical, at page 3, line 23, referring incorrectly to claim 13, rather than the instant claim 21.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5155853	MITSUHIRA	10-1992
5450566	YOSHIDA	9-1995
5751988	FUJIMORA	5-1998
6035422	HOHL	3-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-7, 11, 13-16, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over MITSUHIRA in view of standard register use, as evidenced by YOSHIDA (US 5450566 A).

Regarding claims 1 and 21, MITSUHIRA discloses the register bank blocks (e.g., Fig. 1, "36"), the decoder circuit for activating one of the bank blocks (e.g., Fig. 1, "44") where different interrupt event operations result in selecting different ones of the blocks (e.g., col. 4, lines 39-44). MITSUHIRA also discloses arithmetic operations (e.g., col. 4, lines 9-12) and registers as used for data processing (e.g., col. 1, lines 10-12), but neglects to expressly mention that register data is commonly used in arithmetic operations; however, Examiner takes Official Notice that it is commonplace to perform arithmetic operations on register data, as evidenced by YOSHIDA (e.g., col. 4, lines 45-48). It would have been obvious to one of ordinary skill in the art to combine register contents with the arithmetic operations of MITSUHIRA, because use of registers allows for enhancements, such as efficient use of register addressing modes.

Regarding claim 2, MITSUHIRA also discloses the execution of the first program stream, and executing the second stream associated with an interrupt event (e.g., col. 6, lines 4-9).

Regarding claim 3, MITSUHIRA also discloses the second program stream has higher priority than the first (e.g., col. 5, lines 35-40).

Regarding claims 4 and 5, MITSUHIRA also discloses multiplexing the input data bus by receiving a register bank selection signal coupling the activated register bank block to the input data bus (e.g., col. 6, lines 5-7).

Regarding claims 6 and 7, MITSUHIRA also discloses multiplexing the output data bus by receiving a register bank selection signal coupling the activated register bank block to the output data bus (e.g., col. 6, lines 7-9).

Regarding claim 11, MITSUHIRA also discloses first and second bank blocks are currently enabled and independently addressable (e.g., col. 4, lines 51-54).

Regarding claim 13, MITSUHIRA discloses the register bank blocks (e.g., Fig. 1, "36"), the decoder circuit for activating one of the bank blocks (e.g., Fig. 1, "44"), receiving and determining if an interrupt is to be fulfilled (e.g., col. 6, lines 4-9), and if so selecting a second block isolated from the first ones of the blocks (e.g., col. 4, lines 39-44). MITSUHIRA also discloses arithmetic operations (e.g., col. 4, lines 9-12) and registers as used for data processing (e.g., col. 1, lines 10-12), but neglects to expressly mention that register data is commonly used in arithmetic operations; however, Examiner takes Official Notice that it is commonplace to perform arithmetic operations on register data, as evidenced by YOSHIDA (e.g., col. 4, lines 45-48). It would have been obvious to one of ordinary skill in the art to combine register contents with the arithmetic operations of MITSUHIRA, because use of registers allows for enhancements, such as efficient use of register addressing modes.

Regarding claim 14, MITSUHIRA also discloses the execution of the first program stream, and executing the second stream (e.g., col. 6, lines 4-9).

Regarding claim 15, MITSUHIRA also discloses the second program stream has higher priority than the first (e.g., col. 5, lines 35-40).

Regarding claim 16, MITSUHIRA also discloses the processor (e.g., Fig. 1, "16").

Regarding claim 19, MITSUHIRA also discloses the memory circuit with program stream data (e.g., Fig. 1, "28").

Regarding claim 20, MITSUHIRA also discloses instructions for storing and restoring register bank block contents (e.g., col. 6, line 67 – col. 7, lines 10).

Claims 8-10 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over MITSUHIRA and standard register use, as applied supra, in view of FUJIMURA (US 5751988 A).

Regarding claim 8, MITSUHIRA neglects to expressly mention returning from an interrupt and the need to restore existing conditions; however, this is widely known as seen in FUJIMURA (e.g., col. 2, lines 45-49). It would have been obvious to one of ordinary skill in the art to combine FUJIMURA with MITSUHIRA because FUJIMURA teaches a means to return to the register bank block selection that was interrupted in order to continue operating upon completion of the higher priority processing.

Regarding claim 9, MITSUHIRA also discloses the switching is based on priority (e.g., col. 5, lines 35-40). FUJIMURA teaches the storing upon interrupt (e.g., col. 2, lines 28-32).

Regarding claim 10, MITSUHIRA also discloses the bank signal is solely based on interrupt priority (e.g., col. 5, lines 34-37, all conditions listed considered a prioritization of signal).

Regarding claim 17, MITSUHIRA also discloses selecting the first register block (e.g., col. 5, lines 35-37), halting execution of the second program stream (e.g., col. 16, lines 18-21), but does not expressly mention resuming execution of the first program stream; however this is widely known as seen in FUJIMURA (e.g., col. 2, lines 45-49). It would have been obvious to one of ordinary skill in the art to combine FUJIMURA with

MITSUHIRA because FUJIMURA teaches a means to return to the register bank block selection that was interrupted in order to continue operating upon completion of the higher priority processing.

Regarding claim 18, MITSUHIRA also discloses executing the second program stream does not alter contents of the first register bank block in suspended use (e.g., col. 6, lines 1-3).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over MITSUHIRA and standard register use, as applied supra, in view of standard debugging techniques, as evidenced by HOHL (US 6035422 A).

Regarding claim 12, MITSUHIRA also discloses a register for access to a plurality of bank blocks (e.g., col. 4, lines 51-54), but neglects to mention a step of debugging; however, Examiner takes Official Notice it is widely known to access all register data during debugging as evidenced by HOHL (e.g., col. 34, lines 62-64). It would have been obvious to one of ordinary skill in the art to combine widely known debug techniques to MITSUHIRA because providing full access to operational data during debug maximizes the amount of information to bear on a problem that is being debugged.

(10) Response to Argument

Appellant argues that "Mitsuhira does not disclose "use of special function registers in place of the general registers" and further that Yoshida fails to "cure the deficiency of Mitsuhira". More particularly, Appellant argues that the "special function

registers" intended by Appellant "are accessed by a processor as if they were internal memory", while Mitsuhira's memory "is used to temporarily store a copy of data from program status word (PSW) 20 and program counter 18" which "is then restored to PSW 20 and PC 18 rather than accessed as internal memory".

In point of fact, a processor initiated store and restore of particular data to a memory location can reasonably considered a special function. In particular, it is special because these operations are initiated by an interrupt sequence and not subject to "general" control by the program.

Thus the issue remains, as to whether the memory location to which this data is stored can be considered a register location. Here, Appellant misconstrues Mitsuhira's register banks as being undistinguished from the general memory that contains them. Certainly Mitsuhira teaches the distinction, noting that "the register bank to be accessed by the CPU is switched to the predetermined register bank corresponding to the given interrupt request signal" (col. 2, lines 10-13), and referring to his invention as relating to "a plurality of general register sets ... used for data processing" (col. 1, lines 10-13).

One might argue that Mitsuhira's use of the term "register" is repugnant to its standard use; however, this is not the case. Data memory and register memory are both forms of storing data; what distinguishes the two is in how they are addressed. Virtually all processors distinguish between addressing data in registers from addressing data in general memory. Mitsuhira is no exception; what is novel in Mitsuhira is the use of a plurality of register bank blocks and the means to select which particular block is addressed by the processor when it uses register addressing.

Mitsuhira teaches a means to address general memory, and a means to address a particular register block: "the address decoder 32 decodes an address outputted on the address bus 26 from the CPU 16 to select a corresponding address of the data memory 36. In addition, the address decoder 34 operates to decode a value of the register bank designation register 44 and a *register address* outputted on the address bus 26 from the CPU 16 so as to select on of a plurality of register banks" (col. 4, lines 51-60, emphasis added). There can be no doubt that Mitsuhira employs two distinct addressing modes, one for registers (albeit with a bank select switch), and one for data memory. Mitsuhira recognizes this by referring to the memory addressed by register addresses as registers.

As noted supra, when registers are employed beyond program control to save PC and PSW upon interrupt they are reasonably considered "special function registers"; however, Examiner did not rely on the special designation of registers used to save PC and PSW in the rejection. This is because the claims recited use of "special function registers by the processor during the execution of logical or arithmetic operations". Thus Examiner did not consider the special designation of PC and PSW storage register to be "used" during logical or arithmetic operations. In fact, Mitsuhira generally refers to the remaining registers as "general registers" (see e.g., col. 4, lines 18-21, or col. 1, lines 10-11). For this reason, Examiner used Official Notice to note that it is a widespread practice to designate certain registers as special when conducting logical or arithmetic operations. Yoshida eminently evidences this assertion by providing an example of using a particular register (R2) to receive the result of an arithmetic

calculation. The submission by Appellant of web page entitled "8051 Special Function Register – 8051 Memory – SFR's – 8051 SFR" (submitted as appendix to original Appeal Brief of 4/28/08) also serves this evidentiary purpose, where it designates the use of a register as the accumulator (ACC), and notes it is "one of the most-used SFRs on the 8051 since it is involved in so many instructions" (see page 5, note also that the PSW, explicitly mentioned by Mitsuhira is also referred to as a special register in the evidence supplied by Appellant). Examiner employed Official Notice because it is common to designate a register as having a special purpose for logical or arithmetic functions. Mitsuhira teaches the use of special registers, but neglects to note the use of special registers for arithmetic. The ACC register seen in the Appellant's evidence is a special designation of a register for storing the result of an arithmetic operation which is a legacy of the earliest processors (such as the original Intel 8080 processor) for which abundant evidence (beyond Yoshida and that provided by Appellant) exists. This adequately supports the Examiner's assertion that the use of special registers for arithmetic operations is widely known and employed. If there is a particular distinction between this widely known and even historically employed use of specially designated registers and the Appellant's intended and purportedly distinctive invention, the recitation fails to distinguish despite ample opportunity given the Appellant to provide distinctive recitation.

Appellant further argues that in distinction to Mitsuhira, "Appellant's invention is to facilitate the execution of an interrupting program stream without storing and restoring interrupted program stream critical data... whereas the cited portions of Mitsuhira teach

storing and restoring critical data in response to interrupt requests" (p. 7). However, this distinction is found nowhere in the recited invention. Moreover, Mitsuhira teaches the switching of register banks such that register data does not need to be saved before their use during interrupt processing. Mitsuhira does save the program counter as part of the interrupt procedure so that it can commence fetching of interrupt code; however, this particular operation does not exclude the application of Mitsuhira to the instant claims.

Appellant further argues that Examiner has failed to address "Appellant's explanation of special function registers, without providing any documentary evidence to support such an opinion" (p. 7); however, as noted supra, Appellant's depiction of special function registers is apparently far more narrow than a person of ordinary skill in the art would construe from its recitation in the instant claims. Mitsuhira himself teaches special function registers (noted supra), and as Examiner asserts, special designation of a register specifically in an arithmetic operation is widely employed, which Yoshida adequately evidences, and to which Appellant himself has provided additional evidence in the form of the ACC accumulator register provided in Appellant's evidentiary submission, noted supra.

Appellant further argues that "Examiner admits that Mitsuhira fails to disclose the use of registers for special functions" (p. 8); however, this is incorrect. Examiner noted that Mitsuhira "neglects to expressly mention that register data is commonly used in arithmetic operations" (Final Rejection, communicated 11/29/07, p. 2). As elaborated supra, Mitsuhira certainly teaches the use of special registers, but, following the

recitation, Examiner determined this to be inadequate to anticipate the recited use of "special function registers by the processor *during the execution of the logical or arithmetic operations* [emphasis added]".

Appellant further argues that Examiner argument is that "that one of skill in the art would modify Mitsuhira in view of Yoshida's alleged disclosure of registers that have particular functions" (p. 8). However, this refers incorrectly to grounds of rejection that use Yoshida merely as evidence to the assertion that register data is commonly employed to perform arithmetic operations. As noted previously, and maintained supra, registers are commonly designated to take particular roles in arithmetic operations. Yoshida evidences this, wherein an arithmetic operation is performed using registers (col. 4, lines 45-48). Appellant's own submission evidences this in the more narrow sense of a standard automatic designation of an accumulator register to receive arithmetic results. The evidence of the Examiner assertion of widespread use is abundant beyond these two evidentiary submissions, inasmuch as special designation of registers dates back to the introduction of the Intel 8080 microprocessor in the 70's.

Appellant further argues that "no valid reason has been presented for combining Mitsuhira with Yoshida", and characterizes Examiner as arguing that "Mitsuhira fails to disclose the use of registers for special functions, but argues that one of skill in the art would modify Mitsuhira in view of Yoshida's alleged disclosure of registers that have particular functions" (p. 8). However, as noted supra, Examiner does not combine Mitsuhira with Yoshida in any ground of rejection, nor, as noted supra, does Examiner admit that Mitsuhira fails to disclose the use of registers for special functions. Rather,

Mitsuhira is combined with standard register use asserted by Examiner. Contrary to the Appellant's characterization, Mitsuhira does in fact disclose special register use, namely as storage for PSW and PC data during interrupt; this in fact was specifically noted by Appellant above, although apparently not recognized as a form of specific function. As noted supra and clearly provided in the Final Rejection of 11/29/07, Mitsuhira does not disclose special register use only for the more narrowly recited limitation of use as "during execution of the logical or arithmetic operations." This more narrow deficiency is corrected by Examiner assertion that special designation of a register is widespread. Appellant inadvertently provides evidence of this assertion in his own submission, noted supra.

Appellant argues that "Examiner's modification undermines the operation of the Mitsuhira reference" because Mitsuhira discloses that the register banks are used in a manner that is inconsistent with the use of special function registers" (p. 8). If there is a particular intended limitation to the "special function registers" that would undermine its combination with Mitsuhira, it clearly receives no support in the recitation, despite ample opportunity to amend the claims appropriately. If, on the other hand, Appellant intends by his argument to mean it would be inconsistent to use Mitsuhira's "general registers" for a specific function, then Examiner notes that Mitsuhira already teaches the use of special function registers, namely the PC and PSW save registers, as noted supra. The special designation of registers in this particular case allows for shorter instructions since the particular general register does not need to be explicitly specified in the instruction. This is also the case for the accumulator designation (ACC) in the Appellant

submission of special registers. Because a particular general register takes on the role of accumulator in certain arithmetic operations, the particular register used to accumulate does not need to be specified in the instruction itself. Yoshida presents a more general interpretation where registers can assume certain functions in the course of performing arithmetic operations. If a particular "special function" is intended by Applicant that excludes the standard use of registers for particular roles in arithmetic operations, then this must be positively recited. Appellant has failed to do so.

Regarding claim 8, Appellant argues that it is not clear how the cited references disclose "register bank block selection data indicative of a pre-interrupt state". However, Examiner notes the following: Mitsuhira teaches that routines may be interrupted. In the course of interruption, the current state is superseded by the interrupt state (e.g., col. 4, lines 28-39, and the operation as previously cited e.g., col. 4, lines 39-44). Furthermore, Mitsuhira certainly acknowledges a main "pre-interrupt" operating state ("another register bank 0 used for a main program other than an interrupt handling program" (col. 4, lines 20-21), and he acknowledges the need to return to the main state: "processing, saving and returning to the general registers contents executed in the interrupt handling program" (col. 2, lines 30-32). What Mitsuhira neglects to explicitly teach is that this need is fulfilled, namely a return to the pre-interrupt state. Examiner asserts that this is widely practiced; namely, any design that provides for interrupt processing in a circuit also provides for a return to the state of operations that preceded that interrupt. It is hard to conceive of an interrupting operation that would not provide for normal processing upon the conclusion of the

interrupt. As noted, Mitsuhira acknowledges the need; Mitsuhira provides for the need (in the switched register bank 0, noted supra), all Mitsuhira neglects to do is actually teach the restoring operation. Examiner asserts that this deficiency is common knowledge; Fujimura is merely used as evidence to this assertion. Fujimura provides one of many examples in the literature wherein a pre-interrupt state is saved and then restored. Fujimura states at the cited reference: "At the end of the interruption processing routine, information of the register bank and the memory bank which is to be used in the main routine, which has been stored in the stack area, is restored in accordance with a POP command" (col. 2, lines 45-49). Applicant argues that "Examiner has failed to provide support for: 1) what aspects of the Fujimura reference correspond to the various claim recitations, and 2) how these aspects would function in the asserted circuit of the Mitsuhira reference" (p.9). The cited reference to Fujimura, quoted supra could not make clearer how a pre-interrupt state is restored. Perhaps it needs to be pointed out that "the main routine" in Fujimura can also be considered a "pre-interrupt" routine? It is difficult to see how this could be made any clearer. Regarding the second point, once again, Examiner notes that Fujimura merely provides evidence for an assertion; namely that when a base reference provides a need and provides a means, then actually performing the operation has sufficient motivation. As noted supra, the operation itself (restoring a state of operation after an interrupt) is *widely practiced* and is practically a part of the definition of an interrupt.

Regarding claim 12, Appellant argues that Examiner has failed to support "1) what aspects of the Hohl reference correspond to the various claim recitations; and 2)

how these aspects would function in the asserted circuit of the Mitsuhira reference" (p. 10). Once again, the cited references to Hohl are clear as *evidence*. As to the limitation of providing access to register data during debugging, this is commonly known, and Hohl clearly provides evidence thereto.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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